Refine Search

Search Results -

Terms	Documents
L13 same rout$	1

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L14

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, December 20, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L14	L13 same rout$	1	L14
L13	L11 same l5	22	L13
L12	L11 same l1	1	L12
L11	L3 near3 generat$	421	L11
L10	L3 same generat$	2077	L10
L9	L8 and l1	22	L9
L8	L3 same register	1055	L8
L7	L6 and l1	3	L7
L6	L5 same l3	471	L6
L5	control adj1 signal	559261	L5
L4	L3 and l2	14	L4
L3	test$ near3 path	11294	L3
L2	test$ near3 l1	30	L2
L1	routing near2 resource	1527	L1

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L9: Entry 3 of 22 File: USPT Sep 2, 2003

DOCUMENT-IDENTIFIER: US 6615377 B1
TITLE: Integrated circuit with signal-vector queue for normal and test modes of operation

Brief Summary Text (9):
The problems with loading and noise can be reduced when testing is performed using onboard self-test hardware. However, the capabilities of dedicated self-test hardware are typically limited to conserve integrated circuit area and routing resources for normal functions.

Brief Summary Text (10):
The competition for circuit area and routing resources is less of a concern where testing is performed by a test program run on an onboard processor. However, the test program approach is limited to integrated circuits with suitable processors built in. In any event, a test program is often functionally distant from nodes that it needs to control and observe so that abnormally slow data rates are required for controllability and observability.

Detailed Description Text (20):
Captured-signal nodes 201 and driven-signal nodes 203 are coupled to "normal" signal sources during normal operation through multiplexers. During test-setup mode, captured-signal nodes 201 are coupled to test port 223 so that drive-signal vectors can be written to queue 205. During test-drive mode, driven-signal nodes are coupled to register 217 instead of normal-signal sources to implement the controllability function. In an alternative embodiments, the queue or a register coupled to its input is part of a serial scan chain that provides a path from the test port to store drive vectors in the queue.

Previous Doc Next Doc Go to Doc#

L14: Entry 1 of 1 File: USPT Dec 19, 1995

DOCUMENT-IDENTIFIER: US 5477549 A
TITLE: Cell switch and cell switch network using dummy cells for simplified cell switch test in communication network

Brief Summary Text (25):
According to one aspect of the present invention there is provided a cell switch for switching cells entering from a plurality of input transmission paths to a plurality of output transmission paths according to a routing information indicated in a header of each cell, the cell switch comprising: buffer memory means, connected with the input transmission paths and the output transmission paths, for storing the cells entered from the input transmission paths; buffer memory control means for controlling writing and reading operations with respect to the buffer memory means according to the routing information indicated in a header of each cell; dummy cell generation means for generating dummy cells for a test of the cell switch different from the cells for the data transmission in correspondence to the output transmission paths: and output control means for selectively outputting the dummy cells generated by the dummy cell generation means to the output transmission paths when a test of the cell switch is indicated by an externally provided control signal, and selectively outputting the cells outputted from the buffer memory means to the output transmission paths otherwise.

Brief Summary Text (26):
According to another aspect of the present invention there is provided a cell switch network comprising: a plurality of inter-connected cell switches for switching cells entering from a plurality of input transmission paths to a plurality of output transmission paths according to a routing information indicated in a header of each cell, each cell switch including: buffer memory means, connected with the input transmission paths and the output transmission paths, for storing the cells entered from the input transmission paths; buffer memory control means for controlling writing and reading operations with respect to the buffer memory means according to the routing information indicated in a header of each cell; dummy cell generation means for generating dummy cells in correspondence to the output transmission paths; and output control means for selectively outputting the dummy cells generated by the dummy cell generation means to the output transmission paths when a test of the cell switch is indicated by an externally provided control signal, and selectively outputting the cells outputted from the buffer memory means to the output transmission paths otherwise.

Brief Summary Text (27):
According to another aspect of the present invention there is provided a method of testing a cell switch network formed by a plurality of inter-connected cell switches for switching cells entering from a plurality of input transmission paths to a plurality of output transmission paths according to a routing information indicated in a header of each cell, the method comprising the steps of: (a) equipping each cell switch of the cell switch network with: dummy cell generation means for generating dummy cells in correspondence to the output transmission paths; and output control means for selectively outputting the dummy cells generated by the dummy cell generation means to the output transmission paths when

a test of the cell switch is indicated by an externally provided control signal; (b) inter-connecting the cell switches of the cell switch network in a form of a multi-step configuration; and (c) testing the cell switches belonging to each step in the multi-step configuration of the cell switch network sequentially, by supplying the control signal to each of the cell switches belonging to each step in the multi-step configuration of the cell switch network sequentially, in a reverse order of steps in the multi-step configuration of the cell switch network, starting from the cell switches belonging to a last step in the multi-step configuration of the cell switch network and up to the cell switches belonging to a first step in the multi-step configuration of the cell switch network.

Previous Doc Next Doc Go to Doc#

L7: Entry 2 of 3 File: USPT Mar 24, 1998

DOCUMENT-IDENTIFIER: US 5732246 A
TITLE: Programmable array interconnect latch

Brief Summary Text (4):
2. Ser. No. 08-460,420, now U.S. Pat. No. 5,671,432, BU9-95-023 (0406.152), entitled "PROGRAMMABLE ARRAY I/O-ROUTING RESOURCE";

Brief Summary Text (21):
In a preferred aspect of the present embodiment of this invention, a selective circuit selectively connects the signal storage circuit to either a control signal path or a test control signal path such that the signal storage circuit can be used either for testing or during operation, respectively, of the integrated circuit.

Detailed Description Text (2):
With reference to FIG. 1, there is shown a layout of a programmable gate array 10 comprising a plurality of logic cells. In this particular embodiment, the plurality of programmable logic cells comprises a 56.times.56 array of logic cells divided into sectors 12. Each sector 12 is defined by an 8.times.8 group of logic cells. Also depicted are input/output pins 14 along the perimeter of the array which may be used for data input and output. In addition, certain pins may be dedicated for use as clock pins, reset pins, or for configuration pins for programming the programmable resources of the array 10. The input/output portion of the array can be implemented according to the above-incorporated portions of the U.S. Patent Application entitled "PROGRAMMABLE ARRAY I/O--ROUTING RESOURCE."

Detailed Description Text (26):
In an alternative embodiment of the present invention, multiplexer 108 (as shown in FIG. 12) selectively couples system clocks, of operational control signal paths 112 or test clocks of test control signal paths 110 to the A,B,C inputs 114 of repeater latches 50 of scan chain 51. Accordingly, repeater latches 50.sub.1, 50.sub.2 . . . may be employed during testing of the programmable gate array with appropriate clocking provided by the A,B,C-clocks of test clocks 110. Alternatively, the repeater latches 50.sub.1, 50.sub.2 . . . may be employed together with other logic cells 16 during functional operation of the programmable gate array, latching and processing data per appropriate clocking as provided by system clocks 112.

CLAIMS:

8. An integrated circuit having a plurality of programmable logic cells, a programmable interconnect network for connecting the programmable logic cells, and at least one programmable interface circuit connected within said programmable interconnect network, said programmable interface circuit comprising:

an input node and an output node;

a circuit, connected between said input and output nodes, for selectively providing a buffered output signal to said output node, said buffered output signal being related to a logic state at said input node; and

a signal storage circuit connected to said input node for selectively storing a